CLAIMS:

1. A method for testing digital circuitry through effecting a paired loop-back from a first buffered output to a first buffered input whilst within the circuitry executing at least part of the test through using a **B**uilt-**I**n-**S**elf-**T**est methodology,

characterized by effecting said loop-back from the first buffered data output to a buffered control input.

2. A method for testing digital circuitry through effecting a paired data loop-back from a first buffered output to a first buffered input whilst within the circuitry executing at least part of the test through using a **B**uilt-**I**n-**S**elf-**T**est methodology,

characterized by effecting said loop-back from a buffered control output to the first buffered data input.

3. A method as claimed in Claim 1, characterized by effecting said loop-back from a buffered control output to the first buffered data input.

4. A method as claimed in Claims 1, 2 or 3, whilst in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

5. A method as claimed in Claims 1, 2 or 3, whilst controlling both said loop-back as well as said buffering through a one-bit control signal.

6. A method as claimed in Claim 5, whilst controlling signal routing between said buffering on the one hand, and test circuitry as well as core circuitry of said digital circuitry, on the other hand, through a plural bit control signal.

7. An apparatus arranged for implementing a method as claimed in Claim 1, for testing digital circuitry provided with a paired loop-back from a first buffered output to a first buffered input associated with an in-circuit **B**uilt-**I**n-**S**elf-**T**est facility,

characterized by having said loop-back effected from the first buffered data output to a buffered control input.

8. An apparatus arranged for implementing a method as claimed in Claim 2, for testing digital circuitry provided with a paired data loop-back from a first buffered output to a first buffered input associated with an in-circuit **B**uilt-**I**n-**S**elf-**T**est facility,

characterized by having said loop-back effected from a buffered control output to the first buffered data input.

9. An apparatus as claimed in Claim 7, characterized by having said loop-back effected from a buffered control output to the first buffered data input.

10. An apparatus as claimed in Claims 7, 8 or 9, provided with conversion means for in connection with said buffering executing a conversion between a digital full swing internal signal and an analog low swing external signal with respect to core circuitry of said digital circuitry.

11. An apparatus as claimed in Claims 7, 8 or 9, wherein both said loop-back as well as said buffering have a one-bit control signal input.